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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/715,414	11/17/2000	Kei Nishioka	81876.0018	5571

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EXAMINER	
MICHALSKI, JUSTIN I	

ART UNIT	PAPER NUMBER
2644	7

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/715,414	NISHIOKA, KEI	
	Examiner	Art Unit	
	Justin Michalski	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 4 and 5 are canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yazawa (Japanese Patent JP404339500A) in view of Rao (US Patent 6,665,409).

4. Regarding Claim 1, Yazawa discloses a method of generating surround-sound data including the steps of: providing a memory (Figure 1 RAM) which has sufficient storage capacity for storing a number of bits of data required to maintain a surround-sound for a maximum anticipated delay time (Abstract discloses sampled data is written down in the delay ram and then read out, i.e. delay time). Yazawa further discloses compressing the digital input signal to a compressed digital signal (down-sampling converter) and supplying the signal to memory (delay RAM) and outputting the compressed digital signal from memory and expanding the signal (over-sampling) then adding the digital input signal and the expanded digital signal to output a digital output signal (Figure 1 discloses oversampled signal returning to processor (i.e. added) and then a digital signal outputted). Yazawa does not disclose a delay time adjusting means, or the compression determined based on the instruction delay time and storage

capacity. Rao discloses a method for creating a surround sound signal including a delay buffer (i.e. memory) of a selected length (i.e. delay time) and selected number of taps for taping samples of delay amounts (i.e. capacity) (Paragraph bridging columns 1 and 2). Rao further discloses the compression is determined based on the delay time and storage capacity (Rao discloses different delay time (i.e. storage capacity) is in relation the sampling frequency (i.e. bits) of the device (Column 10, lines 9-16). Rao discloses the advantage of having effect processing supported by the audio decoder chip (Column 1, lines 57-60). Yazawa discloses in the abstract also that it is an advantage that digital processing and delay are done on the same chip. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a delay time adjusting means with the device as disclosed by Yazawa in order to allow a more versatile circuit while still incorporating the device on a single chip.

Regarding Claim 2, Yazawa discloses an apparatus for generating a surround-sound signal from a digital signal input thereto (Figure 1), and providing an output signal derived from said input signal, said apparatus comprising: a memory having a sufficient storage capacity for storing a number of bits of data required to maintain a surround-sound for a maximum anticipated delay time (delay RAM, it is inherent that RAM would have a sufficient amount of storage to function properly), and storing compressed digital signal until said compressed digital signal is retrieved said instruction delay time later (delay RAM); digital compression means for compressing digital input signals to said compressed digital signal (down-sampling) and supplying the compressed digital signal

to said memory (delay RAM); digital expansion means for expanding said compressed digital signal retrieved from said memory (over sampling) said instruction delay time later; and an adder for adding said expanded signal to the current input digital signal (Figure 1 discloses oversampled signal returning to processor (i.e. added) and then a digital signal outputted). Yazawa does not disclose a delay time adjusting means to supply an instruction delay time or compression bits determined based on the instruction delay time and storage capacity. Rao discloses a method for creating a surround sound signal including a delay buffer (i.e. memory) of a selected length (i.e. adjustable time) (Paragraph bridging columns 1 and 2). Rao further discloses the compression is determined based on the delay time and storage capacity (Rao discloses different delay time (i.e. storage capacity) is in relation the sampling frequency (i.e. bits) of the device (Column 10, lines 9-16). Rao discloses the advantage of having effect processing supported by the audio decoder chip (Column 1, lines 57-60). Yazawa discloses in the abstract also that it is an advantage that digital processing and delay are done on the same chip. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a delay time adjusting means with the device as disclosed by Yazawa in order to allow a more versatile circuit while still incorporating the device on a single chip.

Regarding Claim 3, it is well known in the art that digital pulse code modulators are used change the rates of digital signals. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a DPCM for down-sampling and over-sampling as disclosed by Yazawa. (Takegahara et al. US

Patent 5,228,059 is sited to show DPCM use in digital signal expansion and compression).

Regarding Claim 6, Rao further discloses a storage capacity of 5616 samples which provides a 117msec delay at 48Khz (i.e. compression bits) or 127.35 msec at 44KHz. The compression bit can be calculated by dividing the storage capacity by the delay time.

Regarding Claim 7, Rao further discloses having a selected number of taps for tapping samples of corresponding amounts of delay (i.e. can be selected to be step-wise based on the delay time).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin Michalski whose telephone number is (703)305-5598. The examiner can normally be reached on 8 Hours, 5 day/week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Isen can be reached on (703)305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JIM

XU MEI
PRIMARY EXAMINER